

TITLE 1.6T OSFP-RHS Active Loopback Module	DOC No. RFD-20260625300-001	
	REVISION : 01	AUTHORIZED BY : Hawk Rong
	DATE : 2026.06.25	CLASSIFICATION : Optical Transceiver

1. Product Features

- Hot-pluggable 1600G OSFP-RHS Active Loopback
- 3nm CMOS process DSP
- Compliant with OSFP MSA, close top
- VCC voltage ranges from 2.97V to 3.63V
- Operating case temperature 0°C to +85 °C
- Multi-color LED on the front
- The module power distributed to the 3 burners
- Customized CMIS Rev 5.2

2. Product Applications

- Switch aging and testing
- 8x200G, 8x100G ,8x50G active loopback

3. Product Description

3.1 PRODUCT NAME AND SERIES NUMBER(S)

1.6T Active Loopback OSFP-RHS Transceiver

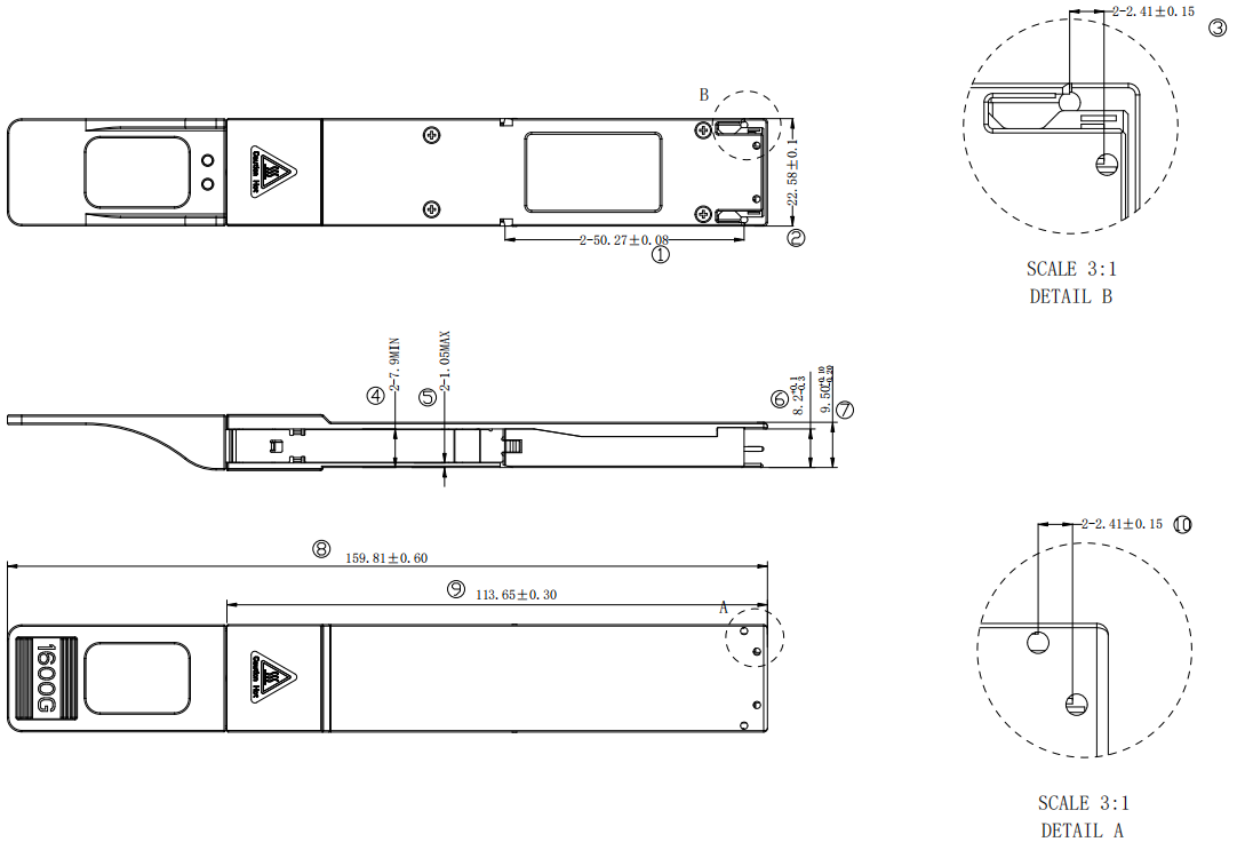
JPC P/N	Bit Rate	Function	Connector	Display
P69**XTKSX00-1	1600G	Active Loopback	NA	Multi-color LED

Notes: ** Indicates the customer code.

3.2 DIMENSIONS, MATERIALS, PLATINGS AND MARKING

The module mechanical design comply with Type 2 in the section 3 of the OSFP Octal Small Form Factor Pluggable Module, Rev 5.0 with power consumption at 50W.

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Unit is millimeter. All dimensions are ± 0.1 mm unless otherwise specified.

3.3 Module Critical Features

The follow are the critical feature requirements for the module and should be consistent with the OSFP MSA.

4. AbsoluteMaximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Supply Voltage	Vcc	-0.3	-	3.6	V	
Storage Temperature	T _s	0	-	+85	°C	
Operating Humidity	RH	5	-	+85	%	
Control Input Voltage	VI	-0.3	-	VCC+0.3	V	

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5. Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T _c	0	-	85	°C	
Power Supply Voltage	V _{cc}	2.97	3.3	3.63	V	
Power Dissipation	P _{diss}	-	-	50	W	
Supply Current	I _{cc}	2	-	16	A	1

Note:

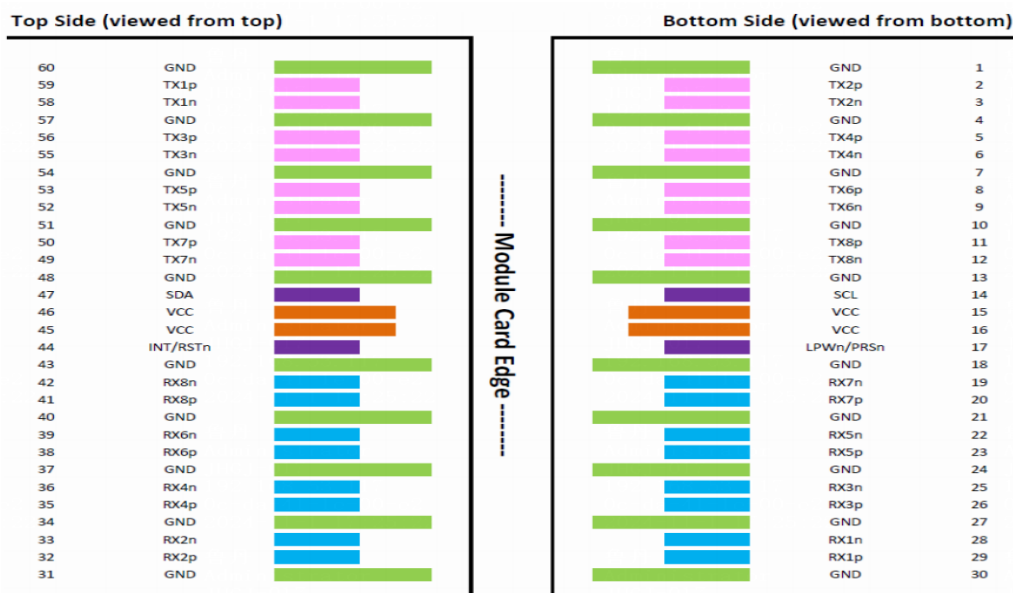
- 1 2A supply current excluding Burners power consumption.

6. Digital Diagnostic Specifications

Parameter	Symbol	Unit	Min	Max	Notes
Temperature monitor absolute error	DMI_Temp	degC	-3	3	Temperature range 0 to 85°C
Supply voltage monitor absolute error	DMI_VCC	V	-10%	10%	Voltage range 2.97 to 3.63V

7. Applications Note:

Pin Definitions



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Pin Function Definitions for OSFP

Pin#	Symbol	Description	Logic	Direction	Plug Sequence
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3
10	GND		Ground		1
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial interface clock	LVC MOS-I/O	Bi-directional	3
15	VCC	+3.3V Power		Power from Host	2
16	VCC	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3
18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3
30	GND		Ground		1

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31	GND		Ground		1
32	RX2p	Receiver Data Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Non-Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Non-Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Non-Inverted	CML-O	Output to Host	3
40	GND		Ground		1
41	RX8p	Receiver Data Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Non-Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3
45	VCC	+3.3V Power		Power from Host	2
46	VCC	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial interface data	LVC MOS-I/O	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Non-Inverted	CML-I	Input from Host	3
50	TX7p	Transmitter Data Inverted	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter Data Non-Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Inverted	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Non-Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Inverted	CML-I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter Data Non-Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Inverted	CML-I	Input from Host	3
60	GND		Ground		1

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8. Programmable power consumption/burner

After power-up, the default power consumption is less than 8W to boot up the DSP, MCU and associated control logic/circuitry. Afterward, host can set the module to consume higher power by programming the 3 burners in 3 regions in section.

9. Memory Map

9.1 00 LowPage Note

Page	Address	Size	Name	Description											
N/A	0	1	Identifier	19h: Identifier Type of OSFP											
	1	1	CmisRevision	53h: CMIS5.3 support											
	2	1	I2C speed	04h: Module supports up to 1 MHz											
	3	1	BIT:7-4 Reserved BIT:3-1 Module state BIT:0 InterruptDeasserted	Reserved Current Module State: <table border="1" style="width: 100%; border-collapse: collapse; margin-left: 20px;"> <thead> <tr> <th style="width: 20%;">Code</th> <th>Module State</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">001b</td> <td>ModuleLowPwr</td> </tr> <tr> <td style="text-align: center;">010b</td> <td>ModulePwrUp</td> </tr> <tr> <td style="text-align: center;">011b</td> <td>ModuleReady</td> </tr> <tr> <td style="text-align: center;">100b</td> <td>ModulePwrDn</td> </tr> <tr> <td style="text-align: center;">101b</td> <td>ModuleFault</td> </tr> </tbody> </table> Status of Interrupt output signal 1b: Interrupt not asserted (default) 0b: Interrupt asserted	Code	Module State	001b	ModuleLowPwr	010b	ModulePwrUp	011b	ModuleReady	100b	ModulePwrDn	101b
Code	Module State														
001b	ModuleLowPwr														
010b	ModulePwrUp														
011b	ModuleReady														
100b	ModulePwrDn														
101b	ModuleFault														
4	1	SumFlagBank0 BIT3: FlagsSummaryBank0Page2Ch BIT2: FlagsSummaryBank0Page14h BIT1: FlagsSummaryBank0Page12h	1b: at least one Flag is set on Bank 0, Page 2Ch 1b: at least one Flag is set on Bank 0, Page 14h 1b: at least one Flag is set on Bank 0, Page 12h												

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		BIT0: FlagsSummaryBank0Page11h	1b: at least one Flag is set on Bank 0, Page 11h
8	1	BIT:6 CdbCmdCompleteFlag1 BIT:0 ModuleStateChangedFlag	Latched Flag to indicate completion of a CDB command for CDB instance 1. Latched Flag to indicate a Module State Change
9	1	BIT:7 VccMonLowWarningFlag BIT:6 VccMonHighWarningFlag BIT:5 VccMonLowAlarmFlag BIT:4 VccMonHighAlarmFlag BIT:3 TempMonLowWarningFlag BIT:2 TempMonHighWarningFlag BIT:1 TempMonLowAlarmFlag BIT:0 TempMonHighAlarmFlag	Latched Flag for low/high supply voltage warning/alarm Latched Flag for low/high temperature warning/alarm
12	2	TempMonValue 2	S16 Module Temperature Monitor (Current Value) internally measured temperature in 1/256 degree Celsius increments
14	2	TempMonValue 1	S16 Module Temperature Monitor (Current Value) internally measured temperature in

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			1/256 degree Celsius increments
16	2	VccMonVoltage	U16 Supply Voltage Monitor (Current Value) internally measured input supply voltage in 100 μV increments
26	1	BIT:7 BankBroadcastEnable BIT:6 LowPwrAllowRequestHW BIT:4 LowPwrRequestSW BIT:3 SoftwareReset	0b: Bank broadcast for lane-banked pages disabled Enables evaluation of the LowPwrRequestHW hardware signal 0b: Module ignores the LowPwrRequestHW signal 1b: Module evaluates the LowPwrRequestHW signal (default) 0b: No request 1b: Request for the module to stay in, or to return into, Low Power mode Self-clearing trigger bit that causes the module to be reset when 1b is written to it. The effect of a SoftwareReset trigger is the same as asserting the Reset hardware signal for the appropriate hold time, followed by its de-assertion. 0b: No action 1b: Software reset (include all)
31	1	BIT:6 CdbCmdCompleteMask1	Mask bit for CdbCmdCompleteFlag1 Mask bit for DataPathFirmwareErrorFlag

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		BIT:2 DataPathFirmwareErrorMask BIT:1 ModuleFirmwareErrorMask BIT:0 ModuleStateChangedMask	Mask bit for ModuleFirmwareErrorFlag Mask bit for ModuleStateChangedFlag
32	1	BIT:7 VccMonLowWarningMask BIT:6 VccMonHighWarningMask BIT:5 VccMonLowAlarmMask BIT:4 VccMonHighAlarmMask BIT:3 TempMonLowWarningMask BIT:2 TempMonHighWarningMask BIT:1 TempMonLowAlarmMask BIT:0 TempMonHighAlarmMask	Mask bit for VccMonLowWarningFlag Mask bit for VccMonHighWarningFlag Mask bit for VccMonLowAlarmFlag Mask bit for VccMonHighAlarmFlag Mask bit for TempMonLowWarningFlag Mask bit for TempMonHighWarningFlag Mask bit for TempMonLowAlarmFlag Mask bit for TempMonHighAlarmFlag

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37	1	CdbStatus1	Refer CMIS 5.3
39	1	ModuleActiveFirmwareMajorRevision	0x00 U8 Numeric representation of the module' s active firmware major revision
40	1	ModuleActiveFirmwareMinorRevision	0x01 U8 Numeric representation of the module' s active firmware major revision
85	1	Module Type Encodings	0x02 (for adaptation switch named 3400)
86	1	ApSelCode 1: Host Electrical Interface Code	0x58 1.6TBASE-CR8
87	1	ApSelCode 1: Module Media Interface Code	0x7F 1.6TBASE-DR8(for adaptation switch,actually is not used)
88	1	ApSelCode 1: Host/Media Lane Count	0x80 Host Lane Count 8,and Media Lane Count 0
89	1	ApSelCode 1: Host Lane Assignment Options	0x01 Start Channel 1 for use this APP
90	1	ApSelCode 2: Host Electrical Interface Code	0x57 800GBASE-CR4
91	1	ApSelCode 2: Module Media Interface Code	0x77 800GBASE-DR4(for adaptation switch,actually is not used)
92	1	ApSelCode 2: Host/Media Lane Count	0x40 Host Lane Count 4,and Media Lane Count 0
93	1	ApSelCode 2: Host Lane Assignment Options	0x11 Start Channel 1 and 5 for use this APP
94	1	ApSelCode 3: Host Electrical Interface Code	0x1F 400GBASE-CR2
95	1	ApSelCode 3: Module Media Interface Code	0x75 400GBASE-DR2(for adaptation switch,actually is not used)
96	1	ApSelCode 3: Host/Media Lane Count	0x20 Host Lane Count 2,and Media Lane Count 0
97	1	ApSelCode 3: Host Lane Assignment Options	0x55 Start Channel 1,3, 5,7 for use this APP

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98	1	ApSelCode 4: Host Electrical Interface Code	0x1E 200GBASE-CR1
99	1	ApSelCode 4: Module Media Interface Code	0x73 200GBASE-DR1(for adaptation switch,actually is not used)
100	1	ApSelCode 4: Host/Media Lane Count	0x10 Host Lane Count 1,and Media Lane Count 0
101	1	ApSelCode 4: Host Lane Assignment Options	0xFF Start Channel 1,2,3,4, 5,6,7,8 for use this APP
102	1	ApSelCode 5: Host Electrical Interface Code	0x49 800G-ETC-CR8 or 800GBASE-CR8
103	1	ApSelCode 5: Module Media Interface Code	0x56 800GBASE-DR8 (for adaptation switch,actually is not used)
104	1	ApSelCode 5: Host/Media Lane Count	0x80 Host Lane Count 8,and Media Lane Count 0
105	1	ApSelCode 5: Host Lane Assignment Options	0x01 Start Channel 1 for use this APP
106	1	ApSelCode 6: Host Electrical Interface Code	0x48 400GBASE-CR4
107	1	ApSelCode 6: Module Media Interface Code	0x1C 400GBASE-DR4(for adaptation switch,actually is not used)
108	1	ApSelCode 6: Host/Media Lane Count	0x40 Host Lane Count 4,and Media Lane Count 0
109	1	ApSelCode 6: Host Lane Assignment Options	0x11 Start Channel 1 ,5 for use this APP
110	1	ApSelCode 7: Host Electrical Interface Code	0x47 200GBASE-CR2
111	1	ApSelCode 7: Module Media Interface Code	0xBF (Reserved value)SMF is not correspondence value(for adaptation switch,actually is not used)
112	1	ApSelCode 7: Host/Media Lane Count	0x20 Host Lane Count 2,and Media Lane Count 0

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113	1	ApSelCode 7: Host Lane Assignment Options	0x55 Start Channel 1,3 ,5,7 for use this APP
114	1	ApSelCode 8: Host Electrical Interface Code	0x46 100GBASE-CR1
115	1	ApSelCode 8: Module Media Interface Code	0x14 100GBASE-DR(for adaptation switch,actually is not used)
116	1	ApSelCode 8: Host/Media Lane Count	0x10 Host Lane Count 1,and Media Lane Count 0
117	1	ApSelCode 8: Host Lane Assignment Options	0xFF Start Channel 1,2,3,4 ,5,6,7 for use this APP
118-121	4	PasswordChangeEntryArea	U32: new password value
122-125	4	PasswordEntryArea	U32: password value
126	1	BankSelect	Refer CMIS 5.3
127	1	PageSelect	Refer CMIS 5.3

9.2 00 HighPage Note

Page	Address	Size	Name	Description
00h	128	1	Identifier	19h: Identifier Type of OSFP
	129-144	16	Vendor name	Vendor name (ASCII)
	145-147	3	VendorOUI	Vendor IEEE company ID
	148-163	16	VendorPN	Part number provided by vendor (ASCII)
	164-165	2	VendorRev	Revision level for part number provided by vendor (ASCII)
	166-181	16	VendorSN	Vendor Serial Number (ASCII)
	182-189	8	DateCode	Manufacturing Date Code (ASCII) Refer CMIS 5.3
	190-199	10	CLEICode	Common Language Equipment Identification Code (ASCII)
	200	1	ModulePowerCtrl	

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		BIT:6 Region 3 burner Enable BIT:5 Region 2 burner Enable BIT:0 Region 5 burner Enable	BIT0, BIT5, and BIT6 control three heating blocks, with 1 turning heating on and 0 turning it off.	
201	1	MaxPower	0x84:MaxPower 33w(for adaptation switch)	
214	1	Region 3 power consumption	Set Value	Heater Level
215	1	Region 2 power consumption	0x10	0
218	1	Region 5 power consumption	0x18	0.72
			0x20	1.0
			0x28	1.5
			0x30	2.0
			0x38	2.5
			0x40	3.0
			0x48	3.5
			0x50	4.0
			0x58	4.5
			0x60	5.0
			0x68	5.5
			0x70	6.0
			0x78	6.5
			0x80	7.0
0x88	7.2			
			0x90	8.0

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				0x98	8.5	
				0xA0	9.0	
222	1		page checksum	Refer CMIS 5.3		
223-255	33		Custom Info	Refer CMIS 5.3		

9.3 01 HighPage Note

Page	Address	Size	Name	Description
01h	128	1	ModuleInactiveFirmwareMajorRevision	0x00
	129	1	ModuleInactiveFirmwareMinorRevision	0x01
	130	1	ModuleHardwareMajorRevision	0x01
	131	1	ModuleHardwareMinorRevision	0x00
	142	1	BIT:6 VDMPagesSupported BIT:5 DiagnosticPagesSupported BIT:2 Page03hSupported BIT1-0: BanksSupported	1b : supported VDM page 20-2F 1b : DiagnosticPages13h-14h supported 1b : User Page 03h supported 00b: Bank 0 supported (8 lanes)
144	1	Maximum duration of the DPDeinit / DPInit state	87h: DPDeinit : 5 s <= T state < 10 s DPInit : 1 s <= T state < 5 s	

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145	1	BIT:7 CoolingImplemented BIT:6-5 TxInputClockingCapabilities BIT:3 ePPSSupported BIT:3 TimingPage15hSupported BIT:2 Aux3MonObservable BIT:1 Aux2MonObservable BIT:0 Aux1MonObservable	0b:Uncooled transmitter device 11b: Lanes may be asynchronous in frequency 0b: ePPS signal processing not supported 0b: Timing characteristics (Page 15h) not supported 0b: Aux 3 monitor monitors Laser Temperature 0b: Aux 2 monitor monitors Laser Temperature 0b: Aux 1 monitor is custom
146	1	ModuleTempMax	5Ah: Maximum allowed module temperature 90°C
147	1	ModuleTempMin	FBh: Maximum allowed module temperature -5°C
150	1	OperatingVoltageMin	94h: Minimum supported module operating voltage 2.9V
151	1	BIT:6-5 RxOutputEqType	00b: Peak-to-peak (p-p) amplitude stays constant, or not implemented, or no information

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153	1	BIT:7-4 RxOutputLevel 3-0 Supported BIT:3-0 TxInputEqMax	0Fh: Amplitude Code 3-0 supported 00h: TxInput Eq is Auto changed, No manual Eq Max value
154	1	BIT:7-4 RxOutputEqPostCursorMax BIT:3-0 RxOutputEqPreCursorMax	0X07:Post-Cursor Equalization 7 dB 0X07:Pre-Cursor Equalization 3.5 dB
155	1	BIT:0 InputPolarityFlipTxSupported	0b: InputPolarityFlipTx control not supported
156	1	BIT:7 BankBroadcastSupported BIT:2 AutoSquelchDisableRxSupported BIT:1 OutputDisableRxSupported BIT0: OutputPolarityFlipRxSupported	0b: The BankBroadcastEnable control is not supported 0b: Host cannot disable automatic squelching of Rx outputs using the AutoSquelchDisableRx register. 1b: Host can disable Rx outputs using the OutputDisableRx register 0b: PolarityFlipRx not supported
157	1	BIT:1	1b: Tx Loss of Signal Flags supported

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		LOSFlagTxSupported BIT:0 FailureFlagTxSupported	1b: Tx Fault Flags supported
159	1	BIT:5 CustomMonSupported BIT:4 Aux3MonSupported BIT:3 Aux2MonSupported BIT:2 Aux1MonSupported BIT:1 VccMonSupported BIT:0 TempMonSupported	1b: Custom monitor supported 0b: Aux 3 monitor not supported 0b: Aux 2 monitor not supported 0b: Aux 1 monitor not supported 1b: Internal 3.3 V monitor supported 1b: Temperature monitor supported
161	1	BIT:6-5 TxInputEqRecallBuffersSupported BIT:4 TxInputEqFreezeSupported BIT:3 TxInputAdaptiveEqSupported BIT:2	00b: Tx Input Eq Store/Recall not supported 0b: Tx Input Eq Freeze not supported 1b: Adaptive Tx Input Eq supported

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		<p>TxInputEqHostControlSupported</p> <p>0b: host-control of Tx Input Eq target not supported</p> <p>BIT:1</p> <p>TxCDRBypassControlSupported</p> <p>0b: If a Tx CDR is supported, it cannot be bypassed</p> <p>BIT:0</p> <p>TxCDRSupported</p> <p>1b: Tx CDR supported supported</p>
162	1	<p>BIT:7</p> <p>VersatileControlSetSupported</p> <p>0b: CMIS-VCS [6] functionality is not supported</p> <p>BIT:6</p> <p>UnidirReconfigSupported</p> <p>0b: ApplyImmediateTx/Rx on Page 10h and DPConfigTx/Rx on Page 19h are not supported</p> <p>BIT:5</p> <p>StagedSet1Supported</p> <p>1b: Staged Control Set 1 supported on Page 10h</p> <p>BIT:4-3</p> <p>RxOutputEqControlSupported</p> <p>11b: both Pre- and Post-cursor supported</p> <p>BIT:2</p> <p>RxOutputAmplitudeControlSupported</p> <p>1b: Rx Output Amplitude control supported</p> <p>BIT:1</p> <p>RxCDRBypassControlSupported</p> <p>0b: Rx CDR Bypass control not supported (if a CDR is supported, it cannot be bypassed)</p> <p>BIT:0</p> <p>RxCDRSupported</p> <p>1b: Rx CDR supported</p>
163	1	<p>CDB Advertisement</p> <p>0x67: Refer CMIS 5.3 for detail</p>

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164	1	CdbReadWriteLengthExtension	0xFF:Refer CMIS 5.3 for detail
165	1	CdbCommandTriggerMethod,and CdbExtMaxBusyTime	0x9F:Refer CMIS 5.3 for detail
166	1	CdbMaxBusySpecMethod , CdbMaxBusyTime	0x80:Refer CMIS 5.3 for detail
167	1	BIT:7-4: MaxDurationModulePwrDn BIT:3-0 MaxDurationModulePwrUp	0X06: 500 ms <= T state < 1 s 0X08: 5 s <= T state < 10 s
168	1	BIT:7-4: MaxDurationDPTxTurnOff BIT:3-0 MaxDurationDPTxTurnOn	0X05: 100 ms <= T state < 500 ms 0X07: 1 s <= T state < 5 s
223	1	ApSelCode 9: Host Electrical Interface Code	0xA0: IB XDR
224	1	ApSelCode 9: Module Media Interface Code	0x73: 200GBASE-DR1 (for adaptation switch,actually is not used)
225	1	ApSelCode 9: Host/Media Lane Count	0x10: Host Lane Count 1,and Media Lane Count 0
226	1	ApSelCode 9: Host Lane Assignment Options	0xFF: Start Channel 1,2,3,4,5,6,7,8 for use this APP
227	1	ApSelCode 10: Host Electrical Interface Code	0xFF: FFh to mark as unused (empty Application Descriptor)
255	1	Page Checksum	The checksum code shall be the low order 8 bits of the arithmetic sum of all byte values from byte 130 to byte 254, inclusive

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9.4 02 HighPage Note

Page	Address	Size	Name	Description
02h	128-129	2	TempMonHighAlarmThreshold	0x5A00: Temp High Alarm 90°C
	130-131	2	TempMonLowAlarmThreshold	0xF600: Temp Low Alarm -10°C
	132-133	2	TempMonHighWarningThreshold	0x5500: Temp High Warning 85°C
	134-135	2	TempMonLowWarningThreshold	0xFB00: Temp Low Warning -5°C
	136-137	2	VccMonHighAlarmThreshold	0x8DCC: Vcc High Alarm 3.63V
	138-139	2	VccMonLowAlarmThreshold	0x7404: Vcc Low Alarm 2.97V
	140-141	2	VccMonHighWarningThreshold	0x875A: Vcc High Warning 3.47V
	142-143	2	VccMonLowWarningThreshold	0x7A76: Vcc High Warning 3.14V

9.5 03 HighPage Note

Page	Address	Size	Name	Description
03h	128-255	128	User Data	Module user data stored in NV memory
	129	1	BIT:7-4 Green Led Status BIT:3-0 Red Led Status	Current LED Status 0000b: Off 0001b:On 00010:Blinking
	138	1	Heater Time Set(Minute)	Set heater time
	139	1	BIT:5 LpMod Control	Read 0b:No edge detected Read 1b:Either rising edge or falling edge crossing the 1.25V thrshold is detected. Write 0b: No effect Write1b: clear the Bit

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			BIT1: LPWn logic status	Read 1b: High Read 0b:Low
	140	1	BIT:1-0 INTL control	0xb:Normal Operation 10b:Force M_INT to logic 0 11b:Force M_INT to logic 1
	168	2	Supply Volatge Size on VccTx	
	170	2	Supply Volatge Size on VccRx	
	174	2	Supply Current Size on VccTx	
	176	2	Supply Current Size on VccRx	
	182	2	Dsp Version	(ASCII) RO

9.6 10 HighPage Note

Page	Address	Size	Name	Description
10h	128	1	Data Path initialization control	Refer CMIS5.3
	138	1	OutputDisableRx<i>	0b: Rx output enabled for lane <i> 1b: Rx output disabled for lane <i>
	143	1	SCS0::ApplyDPInitLane<i>	Refer CMIS5.3
	144	1	SCS0::ApplyImmediate<i>	Refer CMIS5.3
	145-152	8	SCS0::DPConfigLane1-8	Refer CMIS5.3
	162-165	4	SCS0::OutputEqPreCursorTargetRx<i>	Refer CMIS5.3
	166-169	4	SCS0::OutputEqPostCursorTargetRx<i>	Refer CMIS5.3
	170-173	4	SCS0::OutputAmplitudeTargetRx<i>	Refer CMIS5.3
	176	1	SCS0::ApplyImmediateTx<i>	Refer CMIS5.3
	177	1	SCS0::ApplyImmediateRx<i>	Refer CMIS5.3
	178	1	SCS1::ApplyDPInitLane<i>	Refer CMIS5.3
	179	1	SCS1::ApplyImmediate<i>	Refer CMIS5.3
	180-187	8	SCS1::DPConfigLane1 -8	Refer CMIS5.3

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	197-200	4	SCS1::OutputEqPreCursorTargetRx<i>	Refer CMIS5.3
	201-204	4	SCS1::OutputEqPostCursorTargetRx<i>	Refer CMIS5.3
	205-208	4	SCS1::OutputAmplitudeTargetRx<i>	Refer CMIS5.3
	211	1	SCS1::ApplyImmediateTx<i>	Refer CMIS5.3
	212	2	SCS1::ApplyImmediateRx<i>	Refer CMIS5.3
	213	1	DPStateChangedMask<i>	Refer CMIS5.3
	215	1	LOSMaskTx<i>	Refer CMIS5.3
	216	1	CDRLOLMaskTx<i>	Refer CMIS5.3
	232	1	OutputStatusChangedMaskRx<i>	Refer CMIS5.3

9.7 11 HighPage Note

Page	Address	Size	Name	Description
11h	128-131	4	Data Path States	Refer CMIS5.3
	132	1	OutputStatusRx<i>	Refer CMIS5.3
	134	1	DPStateChangedFlag<i>	Refer CMIS5.3
	136	1	LOSFlagTx<i>	Refer CMIS5.3
	137	1	CDRLOLFlagTx<i>	Refer CMIS5.3
	153	1	OutputStatusChangedFlagRx<i>	Refer CMIS5.3
	202-205	4	ConfigStatusLane<i>	Refer CMIS5.3
	206-213	8	ACS::DPConfigLane1-8	Refer CMIS5.3
	223-226	4	ACS::OutputEqPreCursorTargetRx<i>	Refer CMIS5.3
	227-230	4	ACS::OutputEqPostCursorTargetRx<i>	Refer CMIS5.3
	231-234	4	ACS::OutputAmplitudeTargetRx<i>	Refer CMIS5.3

9.8 13 HighPage Note

Page	Address	Size	Name	Description
13h	128	1	Loopback capabilities	0X08: HostSideInputLoopback
	129	1	BIT:7-6 GatingSupport	11b: Supported with time accuracy > 20 ms

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		<p>BIT:5 GatingResultsSupported</p> <p>BIT:4 PeriodicUpdatesSupported</p> <p>BIT:3 PerLaneGatingTimersSupported</p> <p>BIT:2 AutoRestartGatingSupported</p>	<p>1b: Supported</p> <p>1b: periodic update during measurement</p> <p>0b: Only two global gating timers are available for all lanes on all Banks, one for Host Side Measurements and one for Media Side Measurements.</p> <p>1b: AutoRestartGating control (13h:177.4) supported</p>
130	1	<p>BIT:6 HostSideFEC</p> <p>BIT:4 HostSideInputSNRMeasurement</p> <p>BIT:1 BitsAndErrorsCountingSupported</p> <p>BIT:0 BitErrorRatioResultsSupported</p>	<p>1b: Supported (PRBS error information available)</p> <p>1b: Supported</p> <p>1b: Supported</p> <p>1b: Supported</p>
131	1	BIT:3	

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		PRBSGeneratorHostSidePreFEC BIT:1 PRBSCheckerHostSidePreFEC	1b: Supported 1b: Supported
132-133	2	HostSideGeneratorSupportsPattern<i>	0XFF0A Refer CMIS5.3
136-137	2	HostSideCheckerSupportsPattern<i>	0XFF1F Refer CMIS5.3
141	1	BIT:3 HostSideCheckerSupportsDataSwap BIT:2 HostSideCheckerSupportsDataInvert BIT:1 HostSideGeneratorSupportsDataSwap BIT:0 HostSideGeneratorSupportsDataInvert	0b: not supported 1b: supported 0b: not supported 0b: not supported
142	1	BIT:3 HostCheckerSupportsPerLaneEnable BIT:2 HostCheckerSupportsPerLanePattern BIT:1	1b: per lane enable supported 1b: per lane enable supported

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		HostGeneratorSupportsPerLaneEnable BIT:0 HostGeneratorSupportsPerLanePattern	1b: per lane enable supported 1b: per lane enable supported
144	1	HostSideGeneratorEnableLanex	Refer CMIS5.3
148-151	4	HostSideGeneratorPatternSelectLanex	Refer CMIS5.3
160	1	HostSideCheckerEnableLanex	Refer CMIS5.3
161	1	HostSideCheckerDataInvertLanex	Refer CMIS5.3
164-167	1	HostSideCheckerPatternSelectLanex	Refer CMIS5.3
176	1	HostPRBSGeneratorClockSource	0b: All lanes use Internal Clock
177	1	BIT:7 StartStopsIsGlobal BIT:5 ResetErrorInformation BIT:4 AutoRestartGating BIT:3-1 MeasurementTime BIT:0 UpdatePeriodSelect	0b: A start/stop control change acts on current Bank Refer CMIS5.3 Refer CMIS5.3 Refer CMIS5.3 Refer CMIS5.3

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	208	1	PatternCheckGatingCompleteMaskHostLane<i>	Refer CMIS5.3
	212	1	PatternCheckerLOLMaskHostLane<i>	Refer CMIS5.3

9.9 14HighPage Note

Page	Address	Size	Name	Description
14h	128	1	DiagnosticsSelector	Refer CMIS5.3 Supported by 01h,02h,03h,06h
	134	1	PatternCheckGatingCompleteFlagHostLane<i>	Refer CMIS5.3
	138	1	PatternCheckerLOLFlagHostLane<i>	Refer CMIS5.3
	192-255	64	Diagnostics Data	Refer CMIS5.3

9.10 20HighPage Note

Page	Address	Size	Name	Description
20h	128-143	16	VDMDescriptor (Defaule Set SNR (dB) Host Input (Lane 1-8))	Refer CMIS5.3
	144-159	16	VDMDescriptor (Defaule Set PAM4 Level Transition Parameter Host Input (Lane 1-8))	Refer CMIS5.3

9.11 24HighPage Note

Page	Address	Size	Name	Description
24h	128-143	16	eSNR Host Input (Host Lane 1-8)	RO
	144-159	16	PAM4 LTPM Input (Host Lane 1-8)	RO

9.12 2FHighPage Note

Page	Address	Size	Name	Description
2Fh	128	1	BIT:1-0	0b: Group 1 (Page 20h, 24h, 28h, first ¼ of 2Ch, 2Dh)

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			VDMSupport	
	129-130	1	FineIntervalLength	0xC350:interval is 5s

9.13 FFHighPage Note

Page	Address	Size	Name	Description
FFh	250	2	Power-cycle counter	Power-cycle counter. Default to 00_00h from factory.

10. Status LED

A multi-color LED viewed from the front of the module in order to signify high/low power modes, module fully insert, and interrupts:

10.1 LED interface arrangement

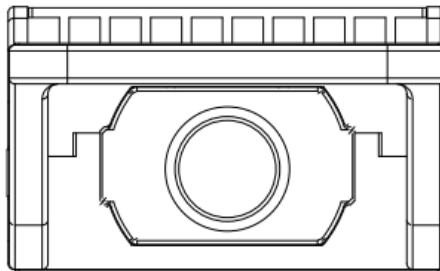


Figure 2 LED interface arrangement

10.2 Inducation of Status Lights

LED	System state	Inducation
Module status	Module is not powered on	OFF
	Module is operating in high power mode	Green (solid)
	Module is operating in low power mode	Orange (solid)
	Module in high pwer mode with voltage or temperature alarm	Green blinking
	Module in low power mode with voltage or temperature alarm	Orange blinking
	Module is in high temperature cut-off fault	Red blinking

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11. Warnings

Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety: Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.

12. Modification History

Rev.	Comments	Date	Originator	Approval
01	Initial	2026.06.25	Hawk Rong	Mike Sun